REMARKS

Claims 1-4, 6-17, 19-53, 55, 57-62, and 64-75 are now pending in the application. Claims 5, 18, 54, 56, and 63 are cancelled without disclaimer or prejudice to the subject matter contained therein. Claim 75 is added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-5, 8-18, 21-26, and 49-74 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jaggar (U.S. Pat. No. 5,701,493). This rejection is respectfully traversed.

With respect to claim 1, Jaggar fails to show, teach, or suggest a register file for a data processing system comprising input ports to receive inputs for addressing at least one register using an encoded address and an address encoder, for each input port, the address encoder to provide an encoded address for accessing one of the plurality of registers. In contrast, Jaggar appears to disclose a single alleged address encoder for all of the input ports of a register.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v.*

Advanced Micro-Devices, Inc., 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Jaggar fails to disclose an address encoder for each input port.

As shown in an exemplary embodiment in FIG. 6, a register file 206 includes a register file memory unit 600 and a plurality of address encoders including, for example, address encoders 602_1, 602_2, 602_3, 602_4, 610_1, and 610_2. Each of the address encoders receives a plurality of inputs. For example, the address encoder 602_1 receives a processor_mode input and a src1.index input. In other words, each of the inputs to the register file memory unit 600 includes a corresponding address decoder.

As best understood by Applicants, Jaggar does not disclose this limitation. For example, with respect to claim 5, the Examiner alleges that Jaggar discloses "**an** address encoder to provider an encoded address" (emphasis added), relying on "the combination of components 12-20 in Fig. 8." Applicants respectfully note that FIG. 8 of Jaggar does not disclose an address encoder for **each** input port as claim 1 recites. Instead, as best understood by Applicants, FIG. 8 of Jaggar discloses a single alleged address encoder (i.e. the components 12-20) for all of the registers.

Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 14, 49, 57, 65, and 69, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

REJECTION UNDER 35 U.S.C. § 103

Claims 27-48 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaggar in view Kerr et al. (U.S. Pub. No. 2003/159021). This rejection is respectfully traversed.

With respect to claim 1, Jaggar, either singly or in combination with Kerr, fails to show, teach, or suggest a register file for a data processing system comprising input ports to receive inputs for addressing at least one register using an encoded address and an address encoder, for each input port, the address encoder to provide an encoded address for accessing one of the plurality of registers. In contrast, Jaggar appears to disclose a single alleged address encoder for all of the input ports of a register.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, the alleged combination fails to disclose the limitation of an address encoder for each input port.

As best understood by Applicants, Jaggar fails to disclose this limitation. As described above with respect to claim 1, the Examiner alleges that Jaggar discloses "**an** address encoder to provider an encoded address" (emphasis added), relying on "the combination of components 12-20 in Fig. 8." Here again, Applicants respectfully note that FIG. 8 of Jaggar does not disclose an address encoder for **each** input port as claim

1 recites. Instead, as best understood by Applicants, FIG. 8 of Jaggar discloses a single alleged address encoder (i.e. the components 12-20) for all of the registers.

Applicants respectfully submit that claim 27, as well as its dependent claims, should be allowable for at least the above reasons. Claim 38, as well as its dependent claims, should be allowable for at least similar reasons.

NEW CLAIM

Applicants added new claim 75. Support for claim 75 can be found throughout the specification, including FIG. 5. As such, no new matter is added.

Applicants respectfully submit that Jaggar, either singly or in combination with Kerr, fails to show, teach, or suggest that each of the plurality of registers has an address having a length of x bits, each of the processor modes has a length of y bits, and the encoded address has a length that is less than x + y bits. For example, Jaggar appears to disclose that the alleged encoded address has a length that is a sum of the lengths of a register address and a processor mode.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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